An Infra-Red Sensitive, Low Noise, Single-Photon Avalanche Diode in 90nm CMOS

Eric A. G. Webster, Justin A. Richardson, Lindsay A. Grant, David Renshaw, Robert K. Henderson

***Abstract*— A Single-Photon Avalanche Diode (SPAD) is reported in 90nm CMOS imaging technology with a peak photon detection efficiency (PDE) of ≈44% at 690nm and better than ≈20% at 850nm. This represents an eight-fold improvement in near infrared sensitivity over existing SPAD structures. This result has important implications for optical communications, time-of-flight ranging and optical tomography applications. The 6.4µm active diameter SPAD also achieves: low dark count rates of typically around 100Hz with ≈51ps FWHM timing resolution; and a low after-pulsing probability of ≈0.375%. The new SPAD structure employs the junction between deep *n*-well and the *p*-substrate rather than being fabricated inside its own well, and is in theory compatible with low-resistivity substrate and thin epi-layer CMOS technology and backside illumination.**

I. Introduction

SINGLE-PHOTON Avalanche Diodes (SPADs) are solid-state photo detectors which utilise the fact that *p*-*n* diodes can be stable for a finite time above their breakdown voltage. When an incident photon with sufficient energy to liberate an electron arrives, avalanche multiplication of the photo-generated electron occurs due to the high electric field. This produces a significant current pulse signalling the time of arrival of a photon which can be detected by CMOS logic.

SPADs were first successfully integrated into a modern small geometry standard CMOS processes in 2003 by A. Rochas [1, 2] using a *p*+-*n*-well SPAD junction with a *p*-well guard ring structure. Devices of this typical SPAD structure have been reported in many generations of CMOS process [3, 4], including 90nm with an *n*+-*n*-well structure [5]. However, devices of the Rochas type in advanced nanoscale CMOS processes have very high doping concentrations on both sides of the active junction which leads to high electric field. Unfortunately, this results in excessive noise due to band-to-band tunnelling which generally gets worse with the increased doping concentrations required by shrinking transistor geometries [5].

A low dark count rate (DCR) SPAD in 130nm was reported in [6] using *p*-well to deep *n*-well (DNW) implants for the active region. A natural guard ring was created by blocking *p*-well around the device periphery and utilising the retrograde doping characteristics of the deep *n*-well implant.

However, thus far, all CMOS SPAD structures have spectral responses which peak in the blue-green region [3, 4, 6]. This is mostly because the active region is formed by shallow junctions between the *p*+ source/drain implants and the *n*-well. Electron-hole pairs generated by long-wavelength photons cannot be sensed as they are formed deep in the substrate beneath the deep *n*-well.

Numerous applications demand high sensitivity in the red and near infrared (NIR) range, for example: range detection, fluorescence lifetime analysis, optical tomography and fibre-optic communications. NIR wavelengths are commonly used in ranging systems because they are invisible. Biological fluorescence lifetime imaging and optical tomography would also benefit because longer light wavelengths cause less cell damage and penetrate deep into tissue. Additionally, an extension of the spectral response allows SPADs to be tailored to different optical fibre transmission windows such as 850nm for glass or 650nm for polymer.

In this paper a SPAD integrated in a 90nm imaging technology achieving a peak detection efficiency of 44% at 690nm using standard implants is reported. To the best of the authors' knowledge, this is the highest PDE achieved in the red by a SPAD in a CMOS process. The reported device is in theory compatible with low-resistivity substrate and thin epi-layer CMOS technology and backside illumination. Additionally, the reported SPAD compares favourably with previously reported structures in other performance areas such as DCR, timing response, and after-pulsing, while being implemented in the most advanced process node [5, 7].

II. Device Structure & CMOS Implementation

The reported SPAD structure, quench component and read-out electronics are fully integrated on-chip. The SPAD is of *n*-type construction, rather than the commonly used *p*-type device inside its own deep *n*-well (DNW) [1-4, 6]. The high field multiplication region is the junction between the deep *n*-well and a thin *p*-epitaxial layer on a low resistivity *p*-substrate. Additionally, *p*-well is placed on top of the active SPAD junction to increase the wavelength selectivity of the detector. The device structure is

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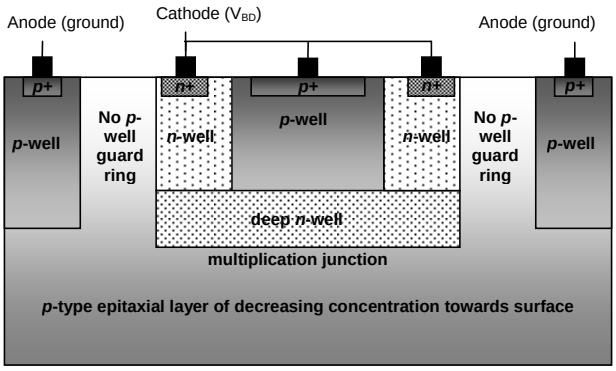

Fig. 1. **Device structure**

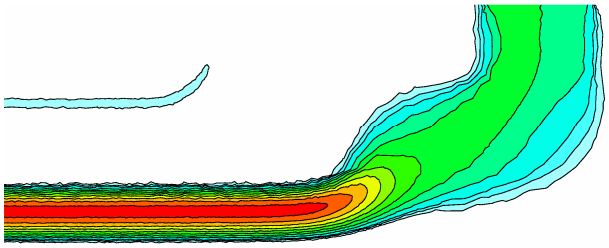

Fig. 2. **Electric field (A.U.) simulation performed with Synopsys Sentaurus TCAD illustrating effectiveness of the new guard ring structure. Red and high contour density indicates high electric field.**

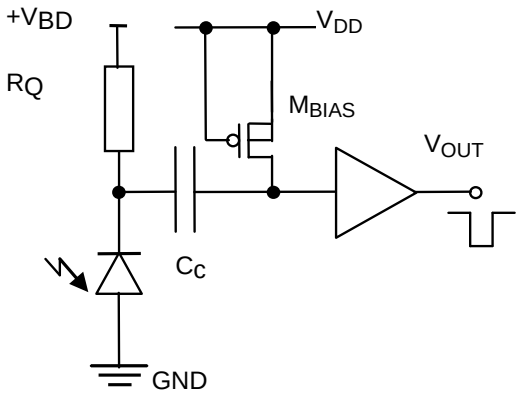

Fig. 3. **CMOS circuit implementation. C_C ≈ 14fF, R_Q≈400kΩ. M_{BIAS} initialises and holds the buffer input voltage.**

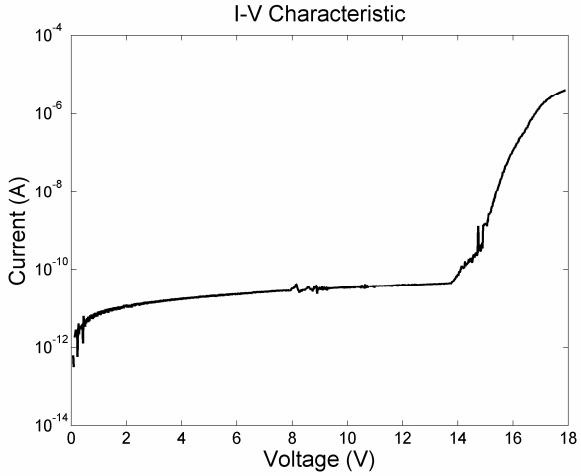

Fig. 4. **I-V Characteristic measured with a HP HP4156B semiconductor parameter analyser illustrating a breakdown voltage of ≈14.9V.**

illustrated in Fig. 1 and has an active diameter of 6.4µm.

The key insight leading to the successful formation of a guard ring was that some CMOS processes are fabricated on an epitaxial layer grown on top of a substrate [8]. In this SPAD structure, the diffusion and implantation characteristics of the *n*-well and DNW implants are used to create the cathode and guard ring. The retrograde DNW concentration increases with depth due to the characteristics of ion implantation while the epitaxial doping concentration in the CMOS process used also increases with depth [8]. The implanted ions then spread and diffuse upwards and outwards creating a lower doped region at the edges which acts as a guard ring; and then *n*-well is implanted on top to enable a contact to be made. Additional novelty in the guard ring structure in a CMOS implementation is the use of a *p*-well blocking layer to create a space between *n* and *p* implants where *p*-well formation is prohibited and the substrate doping profile exists. Moreover, the prohibited *p*-well space is not above a deep *n*-well implant, as in [6], and is adjacent to the biased region of the device. The effectiveness of the guard ring in reducing the electric field around the periphery of the device, without reducing the active area is illustrated in Fig. 2. It is thought that further scaling of this virtual guard ring can be readily achieved to improve the device's fill-factor.

Fundamentally, because this device exists in the substrate the anode terminal is at ground and therefore the positive SPAD breakdown voltage has to be connected to the cathode. However, this high voltage is not compatible with standard CMOS transistors. Therefore, the only efficient method of creating a high voltage compatible 'quench' resistor in CMOS is to use highly resistive polysilicon to connect the cathode of the SPAD to a positive breakdown voltage supply. Moreover, the SPAD cathode, which is the moving node that falls in response to the avalanche current, cannot be directly connected to CMOS gates because it is also at a high DC bias level. Therefore, the SPAD moving node is AC-coupled to subsequent digital CMOS logic to ensure DC compatibility, illustrated in Fig. 3. A two-metal layer metal-oxide-metal (MOM) fringe capacitor is used to implement a high voltage compatible coupling element. The drain-source subthreshold leakage current of an off-PMOS transistor is used to provide the DC bias voltage to the output buffer.

III. Results

The device exhibits a breakdown voltage of ≈14.9V, which is relatively low given the junctions involved, indicating the high well doping concentrations used in nanoscale processes. The I-V curve is illustrated in Fig. 4 obtained with a HP HP4156B semiconductor parameter analyser. Note that the voltage is applied through the quench resistor which leads to the observed shape at high current. The measured reverse bias leakage current is not thought to represent the SPAD leakage current due to the difficulty of measuring ultra-small currents and additional leakage paths.

The spectral response of the SPAD is illustrated in Fig. 5 at three different levels of excess bias, showing a completely different shape to a typical 130nm SPAD structure

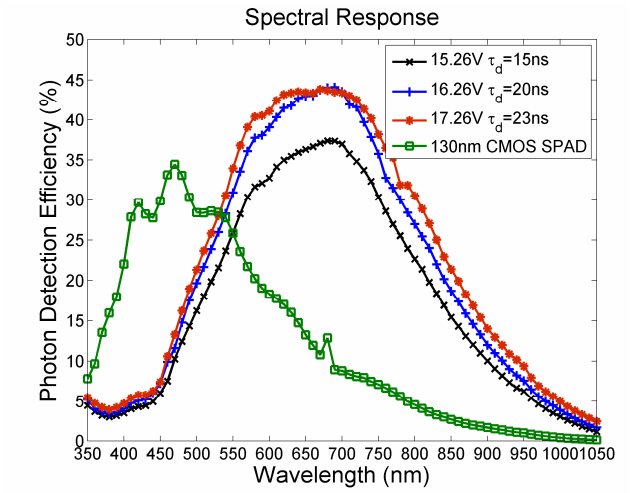

Fig. 5. **Photon detection efficiency of the device operating in Geiger mode at different applied biases and dead times measured at the inverter threshold of 0.6V ($V_{DD}/2$). A traditional SPAD structure implemented in 130nm CMOS is also plotted for comparison purposes [6].**

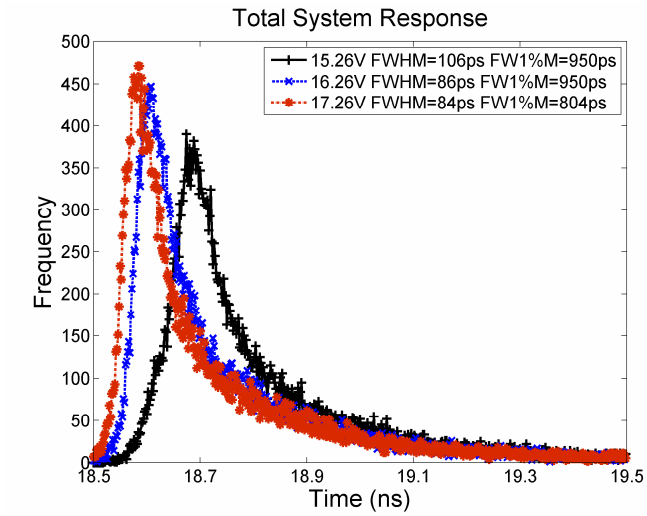

Fig. 6. **The total measured system jitter illustrating an expected timing response improvement with applied voltage. The results include the estimated ≈60ps laser, and ≈30ps output buffer jitters.**

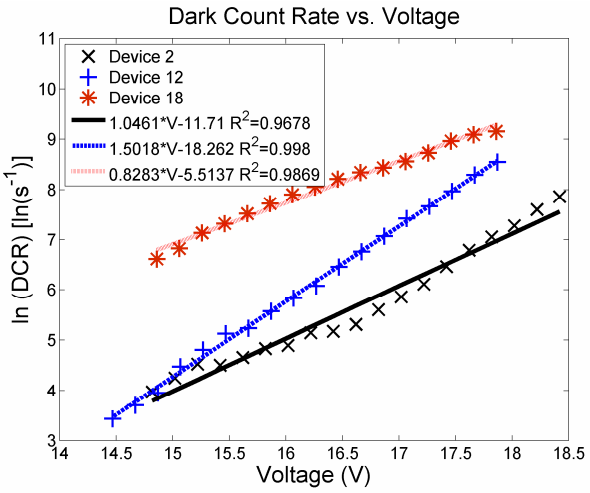

Fig. 7. **Dark Count Rate vs. Voltage plotted for three randomly selected devices. All three devices illustrate an exponential of DCR on applied voltage.**

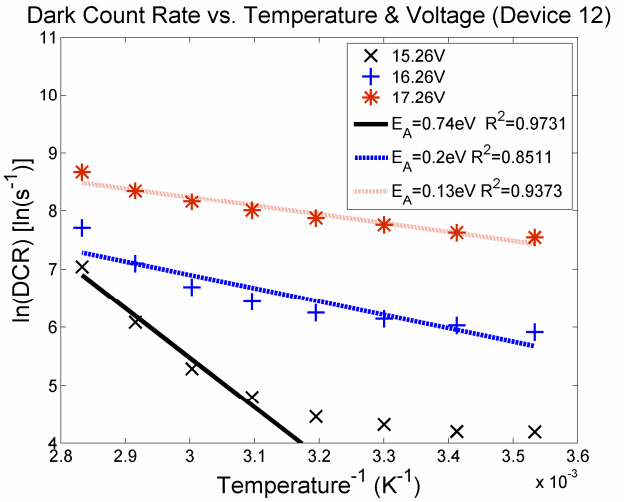

Fig. 8. **Dark Count Rate vs. Temperature at three bias levels plotted for device 12.**

inside its own deep *n*-well [6]. The reduced response in the blue/green region is attributed to the presence of *p*-well on top of the active region. The *p*-well increases the wavelength selectivity of the detector by biasing the spectral response towards red wavelengths, which may be beneficial in some applications. The detector is approximately five times more sensitive to red light and eight times more sensitive to 850nm NIR than existing technology [6].

The timing response of the device was measured with a Picoquant LDH-D-C 470nm pulsed laser with a PDL800D driver. Care was taken to avoid photon pile-up distorting the measurement by attenuating the laser such that the SPAD fired only on less than 5% of laser pulses, indicating single-photon counting. The total system jitter was measured with a LeCroy WavePro 935Zi oscilloscope and is illustrated in Fig. 6 at three bias levels. The measured jitter results include the estimated ≈60ps laser and ≈30ps output buffer chain jitters. Correcting for these additional jitter sources yields SPAD jitters of ≈82ps, ≈53ps, and ≈51ps FWHM at 15.26V, 16.26V, and 17.26V, respectively. The SPAD also shows the expected exponential diffusion tail of a device in the substrate.

The dark count rate of the detector compares favourably with previous CMOS SPADs, showing a typical DCR of ≈100Hz at low excess bias. The DCRs of three randomly selected devices are plotted in Fig. 7 against voltage and all show a strongly exponential dependence, increasing to ≈10kHz at ≈2.4V excess bias on the worst measured device. The trend of DCR against temperature is illustrated in Fig. 8. The low activation energies obtained for ≈1.4 & ≈2.4V excess bias are consistent with band-to-band tunnelling. The 0.74eV activation energy obtained at low excess bias and high temperature is consistent with diffusion and generation current. Moreover, the strong exponential dependence of DCR on applied bias suggests that band-to-band tunnelling is the dominant noise mechanism in the device at room temperature. This is also reasonable given the relatively low breakdown voltage of ≈14.9V, which while high for 130nm and 90nm SPADs [4, 5] is much lower than SPADs manufactured in HV CMOS [2] or fully custom processes [9]. Therefore, the DCR could potentially be improved further by reducing the doping concentration and raising the breakdown voltage. However, this would involve custom fabrication

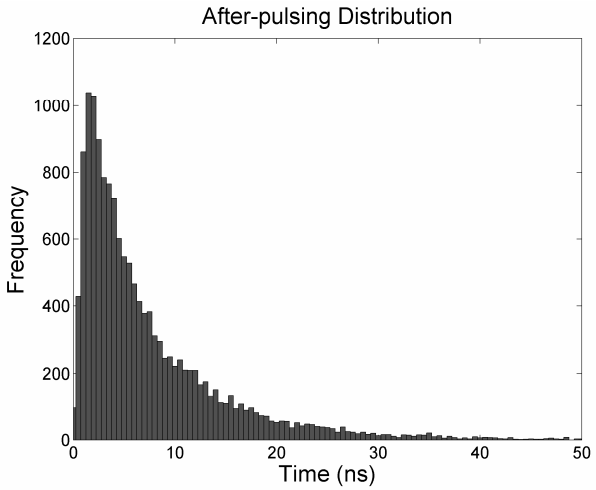

Fig. 9. **Histogram of the measured after-pulsing distribution obtained from four million primary dark count events illustrating a lifetime of ≈8ns.**

steps and generally, advanced CMOS technology is not by default qualified for high voltages.

The after-pulsing of the device was measured by first determining the time-scale of the after-pulsing phenomenon by analysis of the inter-arrival times of dark count events. The observation time was steadily reduced to more accurately observe the deviation from the ideal exponentially distributed poissonian inter-arrival times at short time scales. It was found that the majority of the after-pulsing was contained within 200ns of a primary dark count pulse. With a low DCR of 122Hz at 15.26V, the probability of two dark count events in 200ns is small, $\approx 2.44\times10^{-5}$, and therefore any secondary pulse probability higher than this would be due to after-pulsing.

The oscilloscope was set to measure the time between a primary pulse and a secondary pulse, if one occurred, and left for approximately fourteen hours in the dark. This yielded approximately 4 million primary and 15,000 secondary pulse triggers, giving a total after-pulsing probability of ≈0.375%. This after-pulsing probability again compares favourably with existing standard CMOS SPADs considering the comparatively short dead time of the device [6], and is two orders of magnitude less than previous 90nm SPADs [5]. The exponentially distributed after-pulsing probability obtained with this technique is illustrated in Fig. 9 showing an ≈8ns lifetime.

IV. Conclusion

A CMOS SPAD with what is believed to be record PDE at red and NIR combined with very competitive noise and timing performance in an advanced CMOS process was reported. The SPAD is in theory compatible with triple-well CMOS processes with low-resistivity substrates and thin epi-layer technology. It is also thought that the device is compatible with standard backside illumination imaging processes used to make regular photodiodes and would not require the addition of 'drift rings' [10]. It is believed that the device opens up additional potential applications for SPADs as well as improved performance in existing applications, such as time-of-flight ranging, 3D-cameras and Fluorescence Correlation Spectroscopy. Another potential additional application is in high energy physics where photoelectrons may be generated deep in the substrate or from the back-side and where being able to perform detection and timing integrated in CMOS may be beneficial.

Acknowledgment

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